DIGITAL TWIN LABORATORY · DONG-EUI UNIVERSITY

Measure, model and learn to predict the lifetime of power semiconductors

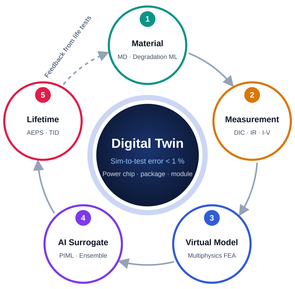
The Digital Twin Lab links material data, in-situ measurement of chips, packages and modules, multiphysics simulation, AI prediction and lifetime assessment into a single digital twin. Each step feeds the next, and life-test results recalibrate the model.

Material → Measure → Model → Learn → Predict

40	34	98	13
Journal papers	Patents	Conference talks	Research projects

01 Research Framework: One Connected Digital Twin

Five research pillars interlock in a loop. Measurement-calibrated models train the AI, the lifetime model verifies the designs the AI finds, and the outcome flows back to material data and testing.

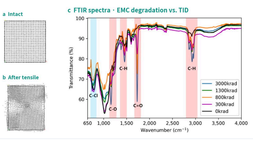


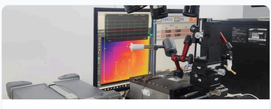
02 From Atoms to Systems

The same digital-twin methodology is applied across length scales. Dot colors show which pillars are used at each scale.

ATOM · nm	CHIP · µm	PACKAGE · mm	MODULE · cm	SYSTEM · m
Atom · Material	**Chip**	**Package**	**Module**	**System**
MD for temperature- and radiation-dependent properties	Equivalent resistivity, conductivity, CTE, layer stresses	TO-220/247/251/252; wire, clip, solder design	Double-side-cooled SiC modules, IGBT benchmarking	MVDC cable ampacity, safe distribution networks

03 Five Research Pillars





02 · MEASURE & CALIBRATE

Measurement-based Calibration

"How does the chip really behave inside the package?"

Chips mounted in open-top ceramic packages are measured with simultaneous DIC, IR thermography and I-V sweeps, exposing strain and temperature that encapsulants normally hide. Equivalent resistivity, thermal conductivity and CTE are then extracted.

< 1 % voltage and temperature error between test and simulation after calibration (15 SiC chips)

Key work · SiC chip CTE via DIC (EuroSimE 2026) · In-situ temperature-strain analysis with open-top packages (KSMPE 2026) · Equivalent properties of SiC PIN diodes (2025) · FEA benchmarking of 8 IGBTs (2025)

01 · MATERIAL

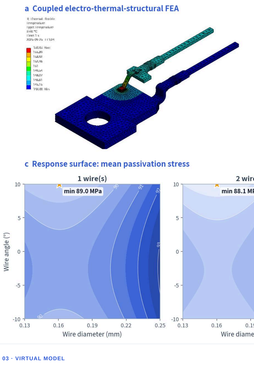
Material Property Data

"Are the inputs to our models right?"

FTIR spectra and machine learning classify thermal and radiation degradation of EMC, SiN and polymers, linked to measured changes in thermal conductivity and hardness. Molecular dynamics (MD) fills in properties the literature does not provide.

0–3000 krad five gamma-ray TID levels of EMC degradation classified from FTIR spectra with machine learning

Key work · EMC TID degradation ML (JEET 2024) · SiN radiation degradation ML+MD (JEET 2025) · FTIR-ANN for 3D-printed polymers (Appl. Sci. 2018–2020) · MD-based pure-Al properties (KSMPE 2026)



03 · VIRTUAL MODEL

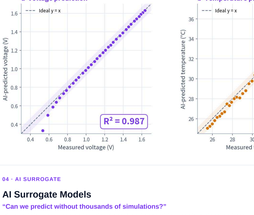
Multiphysics Virtual Model & Design

"Which design variables drive heat and stress?"

Calibrated properties feed coupled electro-thermal-structural-electromagnetic models. Design of experiments and response surfaces then optimize wires, Cu clips, solder, metallization and spacers—for example, mapping passivation-layer stress of a SiC JBS diode against wire diameter, angle and count to find the best bonding condition.

100 → 0 % die-crack rate of a double-side-cooled SiC module eliminated by structural optimization

Key work · Al metallization modeling (Energies 2025) · GaN HEMT packaging DOE/RSM (2025) · Die cracking in DSC SiC modules (2026) · Chip-package interaction of SiC JBS diodes (Energy Reports 2023) · Thermal resistance of hermetic MOSFETs (JEET 2022)



04 · AI SURROGATE

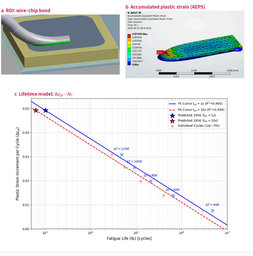
AI Surrogate Models

"Can we predict without thousands of simulations?"

Physics-informed machine learning (PIML) and ensemble models, trained on both measured and simulated data, instantly predict bias-dependent chip properties and package responses (ΔV, ΔT).

$R^2 \geq 0.97$ accuracy of bias-dependent property prediction for 7 IGBTs

Key work · PIML prediction for Cu-clip TO-220 (KCS 2026) · Digital twin for bias-dependent IGBT properties (KCS 2026)



05 · RELIABILITY & LIFETIME

Reliability & Lifetime Prediction

"When and where will it fail?"

Virtual power cycling converts the accumulated equivalent plastic strain (AEPS) at Al-wire interfaces into a lifetime metric, and the model is extended to extreme temperature swings and radiation (TID) environments that are hard to test.

R^2 = 0.96 fit of the AEPS-based Al-wire lifetime model (ΔT 40–195 K)

Key work · AEPS-based Al-wire lifetime model (PHM Korea 2026) · TID degradation of P-MOSFETs (Microelectron. Reliab. 2025) · Wire-bond fatigue in LED packages (Microelectron. Reliab. 2014)

04 How Our Research Evolved

Starting from numerical methods, our work expanded through LEDs and 3D-printed materials to power semiconductors, and now converges into measurement- and AI-driven digital twins.

2010	2014	2017	2020	2023	2026
Numerical methods	**LED package reliability**	**Degradation × ML**	**Power device packages**	**Wide-bandgap devices**	**Measured digital twin + AI**
Implicit-boundary FEM, magnetostatics, inverse analysis	Wire-bond fatigue, silicone degradation, CPI	3D-printed polymers, FTIR-ANN classification	Hermetic/TO thermal resistance, space-grade MOSFETs	SiC/GaN chip-package interaction, TID degradation	Open-top measurement, PIML, AEPS lifetime

05 Where Our Research Goes

Virtual Model Service

Calibrated 3D models and thermal/current results, published per package, to support early design reviews.

View virtual models →

Chip Evaluation & Reliability Testing

Chip-level evaluation and accelerated testing with open-top ceramic packages, DIC, thermal-shock and HTRB equipment.

View equipment →

Design Guidelines & Collaboration

Government and industry projects deliver package design guidelines, lifetime assessment methods and simulation automation.

View projects →